PATENT ABSTRACTS OF JAPAN
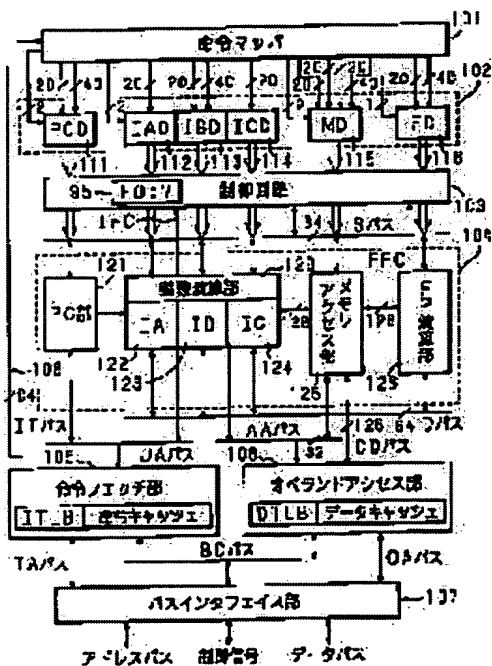
(54) DATA PROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a data processor by which the coding efficiency of an instruction is improved by reducing the requirement of an invalid operation by controlling the number of arithmetic operations and an execution order flexibly by the number of arithmetic fields and a format field to designate the execution order of the arithmetic operation though it is a VLIW type processor fundamentally.

SOLUTION: The arithmetic fields of an instruction code are decoded in parallel by a large number of decoders by reducing the requirement of the invalid arithmetic operation by controlling the number of arithmetic fields of the instruction code and the format field to designate the execution order of the arithmetic operation flexibly, and operating simple decoders 111 to 116 which decode only the arithmetic operation of specific function depending on an arithmetic execution mechanism in parallel. Thereby, the kind of arithmetic operation designated in each arithmetic field is increased, and also, the coding efficiency of the instruction is improved.

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